

BITLINE PRECHARGE TIMING SCHEME TO IMPROVE SIGNAL MARGIN

FIELD OF THE INVENTION

5 This invention generally relates to electronic circuits, and more specifically to nonvolatile semiconductor integrated circuits.

BACKGROUND OF THE INVENTION

10 Nonvolatile memory circuits such as electrically erasable programmable read only memories (EEPROM) and Flash EEPROMs have been widely used for several decades in various circuit applications including computer memory, automotive applications, and video games. Many new applications, however, require the access time and packing density of previous generation nonvolatile memories in addition to low power consumption for battery powered circuits. One
15 nonvolatile memory technology that is particularly attractive for these low power applications is the ferroelectric memory cell. A major advantage of these ferroelectric memory cells is that they require approximately three orders of magnitude less energy for write operations than previous generation floating gate memories. Furthermore, they do not require high voltage power supplies for programming and erasing charge stored on a floating gate. Thus, circuit complexity is reduced and
20 reliability increased.

 The term ferroelectric is something of a misnomer, since present ferroelectric capacitors contain no ferrous material. Typical ferroelectric capacitors include a dielectric of ferroelectric material formed between two closely-spaced conducting plates. One well-established family of
25 ferroelectric materials known as perovskites has a general formula ABO_3 . This family includes Lead Zirconate Titanate (PZT) having a formula $Pb(Zr_xTi_{1-x})O_3$. This material is a dielectric with a desirable characteristic that a suitable electric field will displace a central atom of the lattice. This displaced central atom, either Titanium or Zirconium, remains displaced after the electric field is removed, thereby storing a net charge. Another family of ferroelectric materials is Strontium
30 Bismuth Titanate (SBT) having a formula $SbBi_2Ta_2O_9$. However, both ferroelectric materials suffer

from fatigue and imprint. Fatigue is characterized by a gradual decrease in net stored charge with repeated cycling of a ferroelectric capacitor. Imprint is a tendency to prefer one state over another if the ferroelectric capacitor remains in that state for a long time.

5 A typical one-transistor, one-capacitor (1T1C) ferroelectric memory cell of the prior art is illustrated at Figure 1. The ferroelectric memory cell is similar to a 1T1C dynamic random access memory (DRAM) cell except for ferroelectric capacitor 100. The ferroelectric capacitor (FeCAP) 100 is connected between plateline 110 and storage node 112. Access transistor 102 has a current path connected between bitline 108 and storage node 112. A control gate of access transistor 102 is
10 connected to wordline 106 to control reading and writing of data to the ferroelectric memory cell. This data is stored as a polarized charge corresponding to cell voltage V_{CAP} . Parasitic capacitance of bitline BL is represented by capacitor C_{BL} 104.

 Referring to Figure 2, there is a hysteresis curve corresponding to the ferroelectric capacitor
15 100. The hysteresis curve includes net charge Q or polarization along the vertical axis and voltage along the horizontal axis. By convention, the polarity of cell voltage is defined as shown in Figure 1. A stored "0", therefore, is characterized by a positive voltage at the plateline terminal with respect to the access transistor terminal. A stored "1" is characterized by a negative voltage at the plateline terminal with respect to the access transistor terminal. A "0" is stored in a write operation
20 by applying a voltage V_{max} across the ferroelectric capacitor. This stores a saturation charge Q_s in the ferroelectric capacitor. The ferroelectric capacitor, however, includes a linear component in parallel with a switching component. When the electric field is removed, therefore, the linear component discharges and only the residual charge Q_r remains in the switching component. The stored "0" is rewritten as a "1" by applying $-V_{max}$ to the ferroelectric capacitor. This charges the
25 linear and switching components of the ferroelectric capacitor to a saturation charge of $-Q_s$. The stored charge reverts to $-Q_r$ when the electric field is removed. Finally, coercive points V_C and $-V_C$ are minimum voltages on the hysteresis curve that will degrade a stored data state. For example, application of V_C across a ferroelectric capacitor will degrade a stored "1" even though it is not sufficient to store a "0". Thus, it is particularly important to avoid voltages near these coercive
30 points unless the ferroelectric capacitor is being accessed.

Referring to Figure 3, there is illustrated a typical write sequence for a ferroelectric memory cell as in Figure 1. Initially, the bitline (BL), wordline (WL), and plateline (PL) are all low. The upper row of hysteresis curves illustrates a write “1” and the lower row represents a write “0”.

5 Either a “1” or “0” is initially stored in each exemplary memory cell. The write “1” is performed when the bitline BL and wordline WL are high and the plateline PL is low. This places a negative voltage across the ferroelectric capacitor and charges it to $-Q_s$. When plateline PL goes high, the voltage across the ferroelectric capacitor is 0 V, and the stored charge reverts to $-Q_r$. At the end of the write cycle, both bitline BL and plateline PL go low and stored charge $-Q_r$ remains on the
10 ferroelectric capacitor. Alternatively, the write “0” occurs when bitline BL remains low and plateline PL goes high. This places a positive voltage across the ferroelectric capacitor and charges it to Q_s representing a stored “1”. When plateline PL goes low, the voltage across the ferroelectric capacitor is 0 V, and the stored charge reverts to Q_r representing a stored “0”.

15 A step sensing read operation is illustrated at Figure 4 for the ferroelectric memory cell at Figure 1. The upper row of hysteresis curves illustrates a read “0”. The lower row of hysteresis curves illustrates a read “1”. Wordline WL and plateline PL are initially low. Bitlines BL are precharged low. At time t_0 precharge signal PRE goes low, permitting the bitlines BL to float. At times t_1 and t_2 wordline WL and plateline PL go high, respectively, thereby permitting each
20 memory cell connected to the active wordline WL and plateline PL to share charge with a respective bitline. A stored “1” will share more charge with parasitic bitline capacitance C_{BL} and produce a greater bitline voltage than the stored “0” as shown between times t_2 and t_3 . A reference voltage (not shown) is produced at each complementary bitline of an accessed bitline. This reference voltage is between the “1” and “0” voltages between times t_2 and t_3 . A difference voltage
25 between either a “1” or “0” voltage and a corresponding reference voltage is applied to each respective sense amplifier. The sense amplifiers are activated at time t_3 to amplify the difference voltage. When respective bitline voltages are fully amplified after time t_3 , the read “0” curve cell charge has increased from Q_r to Q_s . By way of comparison, the read “1” data state has changed from a stored “1” to a stored “0”. Thus, the read “0” operation is nondestructive, but the read “1”
30 operation is destructive. At time t_4 , plateline PL goes low and applies $-V_{max}$ to the read “1” cell,

thereby storing $-Q_s$. At the same time, zero voltage is applied to the read “0” cell and charge Q_r is restored. At the end of the read cycle, signal PRE goes high and precharges both bitlines BL return to zero volts or ground. The wordline goes low, thereby isolating the ferroelectric capacitor from the bitline. Thus, zero volts is applied to the read “1” cell and $-Q_r$ is restored.

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Referring now to Figure 5, a pulse sensing read operation is illustrated for a ferroelectric memory circuit. The read operation begins at time t_0 when precharge signal PRE goes low, permitting the bitlines BL to float. Wordline WL and plateline PL are initially low, and bitlines BL are precharged low. At time t_1 , wordline WL goes high, thereby coupling a ferroelectric capacitor to a respective bitline. Then plateline PL goes high at time t_2 , thereby permitting each memory cell to share charge with the respective bitline. The ferroelectric memory cells share charge with their respective bitlines BL and develop respective difference voltages. Here, V_1 represents a data “1” and V_0 represents a data “0”. Plateline PL then goes low prior to time t_3 , and the common mode difference voltage goes to near zero. The difference voltage available for sensing is the difference between one of V_1 and V_0 at time t_3 and a reference voltage (not shown) which lies approximately midway between voltages V_1 and V_0 at time t_3 . The difference voltage is amplified at time t_3 by respective sense amplifiers and full bitline BL voltages are developed while the plateline PL is low. Thus, the data “1” cell is fully restored while plateline PL is low and the data “1” bitline BL is high. Subsequently, the plateline PL goes high while the data “0” bitline BL remains low. Thus, the data “0” cell is restored. The plateline PL goes low at time t_4 , and precharge signal PRE goes high at time t_5 . The high level of precharge signal PRE precharges the bitlines to ground or V_{ss} . The wordline WL goes low at time t_6 , thereby isolating the ferroelectric capacitor from the bitline and completing the pulse sensing cycle.

Turning now to Figure 6, there is a simplified diagram of an unselected ferroelectric memory cell of the prior art illustrating a problem with both step and pulse sensing schemes. Here, the same reference numerals are used as in the memory cell of Figure 1 to show comparable elements of the ferroelectric memory cell. Resistor R_{GATE} 114 represents subthreshold leakage path of access transistor 102. Diode 116 is a parasitic junction diode between storage node 112 and the memory circuit substrate. The wordline terminal WL 106 is adjacent a selected wordline (not

shown) during a read operation. Thus, wordline terminal 106 may develop 200 mV during a low-to-high transition of the adjacent active wordline, as will be explained in detail. Plateline 110 is common to cells on the selected wordline as well as the unselected cell. Ferroelectric capacitor 100 stores a respective data signal and preferably has zero volts until a coercive voltage is developed across the terminals as previously explained. For the following exemplary discussion, ferroelectric capacitor 100 has approximately 30 fF capacitance.

During a read or write operation a selected wordline adjacent wordline WL 106 is driven high to approximately 2.2 V. This capacitively couples 200 mV to wordline terminal 106 and greatly increases subthreshold conduction of access transistor 102. Bitline BL 108 is driven low, and plateline PL 110 is driven high to approximately 1.65 V. Due to charge sharing with diode 116 and gate-to-source capacitance of access transistor 102, the plateline PL transition couples 1.6 V to storage node 112. Thus, storage node 112 goes from 0 V to 1.6 V. Under these conditions at high temperature, subthreshold leakage current I_{SUB} of access transistor 102 increases from less than 1 nA when there is no coupling to wordline 106 to approximately 100 nA, or about two orders of magnitude, when 200 mV is coupled to wordline 106. This level of subthreshold leakage current through resistor R_{GATE} 114 lasts for approximately 4 ns until the wordline drive circuit can restore wordline WL 106 to 0 V. The subthreshold current I_{SUB} of 100 nA for 4 ns, however, represents a 13 mV decrease in storage node voltage subject to the previously described conditions. Moreover, this charge loss is cumulative. Minimal current flows from bitline BL 108 through access transistor 102 when plateline PL 110 returns to 0 V due to the small drain-to-source voltage. Subsequent memory accesses to memory cells adjacent wordline WL 106 and resulting charge loss, however, may result in a negative voltage of as much as -200 mV at storage node 112. Such memory accesses would significantly degrade the data "1" level of the ferroelectric memory cell resulting in read errors. This degradation of the data "1" level introduces a bitline voltage imbalance and may even depolarize the ferroelectric capacitor.

SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the invention, a memory circuit and method to improve signal margin is disclosed. The circuit includes a memory array arranged in rows and columns of memory cells. Each row of memory cells is connected to a respective wordline. Each column of memory cells is connected to one of a bitline and a complementary bitline. An active wordline accesses a respective row of memory cells. The memory circuit includes a plurality of precharge circuits. Each precharge circuit is connected to a respective column of memory cells and coupled to receive a precharge signal. An active precharge signal renders a respective precharge circuit conductive. A control and decode circuit produces an active wordline signal while the precharge signal is active and before a plateline signal is activated. This active precharge signal eliminates accumulated charge at each memory cell storage node, thereby improving signal margin.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the present invention may be more fully understood from the following detailed description, read in conjunction with the accompanying drawings, wherein:

Figure 1 is a circuit diagram of a ferroelectric memory cell of the prior art;

Figure 2 is a hysteresis curve of the ferroelectric capacitor 100 of Figure 1;

Figure 3 is a timing diagram showing a write operation to the ferroelectric memory cell of Figure 1;

Figure 4 is a timing diagram of a step sense read operation from the ferroelectric memory cell of Figure 1;

Figure 5 is a timing diagram of a pulse sense read operation from the ferroelectric memory cell of Figure 1;

Figure 6 is a simplified circuit diagram of the prior art showing charge accumulation at the ferroelectric memory cell storage node due to subthreshold leakage;

Figure 7 is a schematic diagram of an embodiment of the memory circuit of the present invention;

Figure 8A is timing diagram of a first embodiment of the memory circuit of the present invention; and

Figure 8B is a timing diagram of a second embodiment of the memory circuit of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to Figure 7, there is a memory circuit of the present invention. Although the memory circuit includes many similar memory arrays, only a portion of one array is shown for clarity. The memory array includes memory cells arranged in rows corresponding to wordlines 702, 704, 706 and columns 750, 752. Individual memory cells are indicated by circles at intersections of rows and columns. In an embodiment of the present invention there are preferably 512 rows and 64 columns in the memory array. The memory array also includes 16 platelines 710-718. Each plateline is coupled to receive a respective plateline signal PL_0 - PL_{15} . Each plateline, for example plateline 710, is common to 32 rows of memory cells including rows common to wordlines 702-706. Each row of memory cells is selected by an active wordline signal. For example, row 704 is selected by active wordline signal WL_X on wordline 704. Each column includes a bitline 708 and a complementary bitline 709 that form a bitline pair. Each bitline pair is coupled to a respective sense amplifier such as sense amplifier 730. Each sense amplifier has complementary output terminals coupled to local input/output lines LIO 746 and /LIO 748 by column select transistors 742 and 744, respectively. The column select transistors are selected by an active column select signal, for example, YS_Y on lead 740. Each column has a respective precharge circuit including first 724, second 726, and third 728 precharge transistors. The first and second precharge transistors respectively couple the bitline 708 and complementary bitline 709 to voltage terminal GND via lead 722 in response to an active precharge signal PRE on lead 720. A third precharge transistor couples the bitline 708 and complementary bitline 709 to each other in response to the active precharge signal PRE on lead 720.

In operation, the control and decode circuit 700 receives a chip enable signal CE, an address signal A_N including N address bits, and a read/write signal WR. The control and decode circuit produces an active wordline signal WL, an active column select signal YS, an active plateline signal PL, and a precharge signal PRE, where WL, YS, and PL represent a respective group of wordlines, column select lines, and platelines. A selected memory cell at the intersection of the addressed row and column receives or produces data on a respective bitline in response to a logical state of read/write signal WR. For example, when read signal WR is high, a write operation is

performed. Alternatively, when read/write signal is low, a read operation is performed. For either a read or a write operation, when a wordline signal such as wordline signal WL_X goes active high, a small voltage is coupled to adjacent wordlines WL_{X+1} 702 and WL_{X-1} 706 through fringe capacitors CF 770 and 772, respectively. This capacitive coupling increases the voltage on the adjacent wordlines WL_{X+1} 702 and WL_{X-1} 706 by as much as 200 mV and increases subthreshold leakage by approximately two orders of magnitude. Next, a low-to-high transition of plateline signal PL_0 710 induces subthreshold current to flow from the storage node to the bitline. This charge loss couples as much as -13 mV to the storage node of each memory cell along adjacent wordlines 702 and 706 following a subsequent high-to-low transition of plateline signal PL_0 710. Moreover, the subthreshold current from bitline to storage node of the memory cells on adjacent wordlines 702 and 706 when plateline signal PL_0 is low is much less than when high as previously explained. This is because the drain-to-source voltage of each access transistor is much less. Thus, repeated access to wordline WL_X 704 results in accumulated negative voltage of as much as -200 mV at the storage node of each memory cell on adjacent wordlines 702 and 706.

Referring to Figures 7 and 8A, a step sensing read or write memory cycle will be described in detail. In the following description, a memory cycle is from time t_0 through time t_6 . The memory cycle on an adjacent wordline, for example wordline 702, is initiated when wordline signal WL_{X+1} goes active high at time t_0 . This turns on access transistor 102 (Figure 6) while precharge signal PRE remains high and precharge transistors 724, 726, and 728 are still on. Due to the relatively small negative charge at storage node 112, a voltage of wordline signal WL_{X+1} slightly greater than the threshold voltage of access transistor 102 is adequate. Likewise, a voltage of precharge signal PRE slightly greater than the threshold voltage of precharge transistors 724 and 726 is adequate. Storage node 112 is charged through access transistor 102 and complementary bitlines 708 and 709 are equalized through precharge transistor 728, thereby eliminating accumulated negative voltage. This elimination of accumulated negative voltage is highly advantageous. Complementary bitlines are fully equalized prior to sensing and signal margin is not degraded, therefore, by a bitline voltage imbalance.

Next, precharge signal PRE goes low at time t_1 and turns off precharge transistors 724, 726, and 728. Then plateline signal PL_0 goes active from an inactive state at time t_2 . The high level of plateline signal PL_0 exceeds the coercive voltage V_C (Figure 2) of the ferroelectric capacitor and develops a voltage on bitline 709 representing one of a data “1” or a data “0”. Bitline 708 receives a reference voltage intermediate the data “1” and data “0” levels, thereby producing a difference voltage at the input/output terminals of sense amplifier 730. At time t_3 , sense amplifier 730 is activated to develop either a full data “1” or data “0” level on bitline 709. If a data “0” is developed on bitline 709, the memory cell ferroelectric capacitor is restored while the plateline signal PL_0 is high and bitline 709 is low. Alternatively, if a data “1” is developed on bitline 709, the memory cell ferroelectric capacitor data is destroyed as previously explained with respect to Figure 4. At time t_5 , plateline signal PL_0 goes low. This low level of plateline signal PL_0 and high level of a data “1” bitline 709 restores the memory cell ferroelectric capacitor data. Precharge signal PRE returns to a high level at time t_4 , thereby turning on precharge transistors 724, 726, and 728 and precharging complementary bitlines 708 and 709 to ground GND through lead 722. The memory cycle is completed when wordline signal WL_{X+1} goes low and turns off respective access transistors along wordline 702.

Referring now to Figures 7 and 8B, a read or write memory cycle for a pulse sensing circuit will be described in detail. In the following description, a memory cycle is from time t_0 through time t_8 . Adjacent wordline signal WL_{X+1} 702, for example, goes active high at the beginning of a memory access cycle at time t_0 . As in the previous discussion, access transistor 102 (Figure 6) turns on while precharge signal PRE remains high and precharge transistors 724, 726, and 728 are still on. Due to the relatively small negative charge at storage node 112, a voltage of wordline signal WL_{X+1} slightly greater than the threshold voltage of access transistor 102 is adequate. Likewise, a voltage of precharge signal PRE slightly greater than the threshold voltage of precharge transistors 724 and 726 is adequate. Storage node 112 (Figure 6) is charged through access transistor 102 and complementary bitlines 708 and 709 are equalized through precharge transistor 728, thereby eliminating accumulated negative voltage. Thus, any accumulated negative voltage (or positive voltage for any reason not described above) at the sense node is eliminated and complementary

bitlines are fully equalized prior to sensing. Signal margin, therefore, is not degraded due to bitline imbalance.

Next, precharge signal PRE goes low at time t_1 and turns off precharge transistors 724, 726, and 728. Then plateline signal PL_0 goes active from an inactive state at time t_2 . The high level of plateline signal PL_0 exceeds the coercive voltage V_C (Figure 2) of the ferroelectric capacitor and develops a voltage on bitline 709 representing either a data "1" or a data "0". Bitline 708 maintains a reference voltage intermediate the data "1" and data "0" levels, thereby producing a difference voltage at the input/output terminals of sense amplifier 730. At time t_3 , plateline signal PL_0 goes low and returns the common mode bitline voltage to near zero. The difference voltage available for sensing is the difference between one of voltages V_1 and V_0 at time t_3 and a reference voltage (not shown) which is approximately midway between voltages V_1 and V_0 at time t_3 . At time t_4 , sense amplifier 730 is activated to develop either a full data "1" or data "0" level on bitline 709. If a data "1" is developed on bitline 709, the memory cell ferroelectric capacitor is restored while the plateline signal PL_0 is low and bitline 709 is high. Alternatively, if a data "0" is developed on bitline 709, the memory cell ferroelectric capacitor is restored at time t_5 after the plateline signal PL_0 goes high and while bitline 709 is low. At time t_6 , plateline signal PL_0 goes low again. This low level of plateline signal PL_0 and high level of bitline 709 provides additional time to restore a data "1" memory cell ferroelectric capacitor between times t_6 and t_7 . Precharge signal PRE returns to a high level at time t_7 , thereby turning on precharge transistors 724, 726, and 728 and precharging complementary bitlines 708 and 709 to ground GND or V_{ss} through lead 722. The memory cycle is completed when wordline signal WL_{X+1} goes low and turns off respective access transistors along wordline 702.

The present invention advantageously eliminates accumulated negative or positive voltage at the storage node of ferroelectric memory cells prior to either step sensing or pulse sensing. Bitlines and complementary bitlines are precharged to a predetermined voltage until immediately before sensing. Other forms of array noise, therefore, are reduced. Any accumulated negative or positive voltage at the storage node is not imparted to the bitline difference voltage. Thus, signal margin is improved prior to sensing.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, referring back to Figures 7, 8A, and 8B, column select signal YS_Y on lead 740 may be activated any time between times t_2 and t_4 during a write operation. Such timing variations depend on sense amplifier design and individual design preference. Furthermore, a preferred embodiment of the present invention has been described with respect to a one-transistor/one-capacitor (1T/1C) storage cell.

The present invention, however, is equally applicable to two-transistor/two-capacitor (2T/2C) memory cells. These 2T/2C cells are complementary 1T/1C memory cells. A wordline (or wordlines) activates the 2T/2C memory cell, thereby coupling the complementary 1T/1C memory cells to their respective complementary bitlines. If the 2T/2C memory cell stores a data "1", for example, the true and complementary bitline voltages change to produce a total difference voltage.

The present invention with the previously described timing of Figures 8A and 8B would advantageously eliminate bitline imbalance due to storage node voltage accumulation as with the previously described embodiments. It is therefore intended that the appended claims encompass any such modifications or embodiments.